## REMARKS / ARGUMENTS

In response to the Office action dated July 6, 2004 ("OA"), Applicant respectfully requests the Office to consider the following remarks. By this response, no amendments have been made, and no claims have been added. Claims 3-8, 10-15 and 17-26 remain pending in this application.

In the Office action, the Examiner rejected claims 3-8, 10-15 and 17-26 under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent No. 5,115,506 to Cohen et al. ("Cohen").

35 U.S.C. § 102(b) Rejection

Claims 3-8, 10-15 and 17-26 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Cohen. *See* OA, page 2 ¶ 3.

In direct contradiction to the Office's first characterization, the Examiner now presents a new interpretation of Cohen:

> After carefully reviewed Cohen's reference [sic.], Examiner found Cohen does disclose "wherein a portion of said exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls." And "wherein servicing said exception using said at least one set of exception registers comprises modifying the values of the registers in said exception registers without disrupting the state of the interrupt task." As Cohen notes at col. 3, lines 8-28, wherein data register D2(exception registers) can be implemented as a source of operation (service operating system calls) or destination of an operation (servicing interrupts); and wherein transparent implies without disruption [sic.] the state)

OA, pg. 11, ¶ 4.

However, Cohen fails to teach or suggest, inter alia, a set of exception registers "wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls," as recited in independent claims 6, 12, 17, 20 and 23. Claim 14 contains similar language specifying such portioning for the exception registers, and thus is also distinguished from Cohen for the reasons stated below. In particular, the portions of Cohen cited by the Examiner (col. 3, lines 8-28) fail to teach or suggest the exception register allocation called for by such claim language; nor is this deficiency overcome by the remainder of Cohen. Thus, Cohen cannot anticipate claims 6, 12, 14, 17, 20 and 23 under 35 U.S.C. § 102.

As an initial matter, Applicant respectfully submits that the Office has not adequately articulated how the register cited against these claims ("data register D2(exceptional register)"; OA, pg. 11, ¶ 4) corresponds to the "set of exception registers." Though again unclear, the Office's position appears to be either that both occurrences of "data register D2" anticipate the "set of exception registers," or that this term is anticipated by one of the occurrences. Both of these positions are refuted below; however, Applicant's position here is made *in arguendo* due the Office Action's failure to state a definitive position .

One possible position of the Office is that one of the occurrences of "data register D2" (e.g., D2 from either normal register set 16 or alternate register set 18) anticipates the "set of exception registers." However, this position is untenable. As an initial matter, any one of the "data register D2" elements, alone, is simply an

individual register. Thus, this use of "data register D2" would refer to a singular register, which cannot be argued to anticipate a "set" of registers. It is also unclear whether the Office, in the instant hypothetical, is using "data register D2" from the normal register set 16, or from the alternate register set 18. Hence, this position, if it were even articulated, fails to set forth a "set of exception registers" and thus cannot possibly anticipate the claims.

Moreover, the failure to identify the precise "data register D2" that is compared to the claims prevents any clear issue from being developed between the Examiner and Applicant (see MPEP § 706.07), and forces Applicant to speculate. If, for example, the Office is arguing that "data register D2" allocation mentioned in association with normal register set 16 anticipates these claims, it would then be appropriate for Applicant to point out that "data register D2" is not an "exception register" because, e.g., "normal register set 16" is not a "set of *exception* registers." Therefore, Cohen fails to teach or suggest the above-recited claim language as possibly suggested by the Examiner.

With respect to the position that both occurrences of "data register D2" anticipate the "set of exception registers," other deficiencies are present. Applicant notes that the Office, here, would be trying to arbitrarily group together the "data register D2" elements that exist in two *different* register sets (i.e., normal register set 16 <u>and</u> alternate register set 18). If this were the Office's position, it would then be inappropriate for the Office to argue that Cohen somehow allocates a "*portion* of *said set* of exception registers" to servicing interrupt and another "portion" of "<u>said</u>

set" to servicing operator system calls. Clearly, the "data register D2" element used in this manner would be composed of registers from two different sets. However the claims clearly mandates that both portions are of the same "set" ("said set"). If the Examiner is comparing the registers in this manner, such use fails to anticipate claim language reciting that *two* portions of *one* set were allocated for different uses. Thus, any attempt by the Office to argue that both "data register D2" elements anticipate the "set of exception registers" also fails.

Applicant respectfully disputes other characterizations made by the Office, such as the apparent position that the "source of operation" (OA, sentence bridging pp. 11-12, which presumably corresponds to the "source of an operand" language from col. 3, line 19 of Cohen) somehow anticipates "another portion of said set of exception registers is for servicing operating system calls," if that is indeed what the Examiner is arguing. However, Applicant has sufficiently indicated Cohen's deficiencies, above, and thus no further argument is necessary. Therefore, it is respectfully submitted that independent claims 6, 12, 14, 17, 20 and 23 are allowable over Cohen under 35 U.S.C. § 102(b). Similarly, claims 3-5, 7-8, 10, 13, 15, 18-19, 21-22 and 24-26 depend from these independent claims, and are allowable for at least the same reasons. Accordingly, it is respectfully submitted that the instant rejection to claims 3-8, 10, 12-15, 17-26 be withdrawn.

Moreover, because no clear issue has been developed (see MPEP § 706.07), Applicant respectfully requests that the subsequent Office action in this case not be made final. If, however, the Primary Examiner believes that such

action may appropriately be deemed final, Applicants would further respectfully request the opportunity to conduct a telephonic interview with the Examiner(s) prior to issuing such action, so that the Office's position might thereby be clarified and responsive arguments and/or amendments presented.

Cohen also fails to teach or suggest, inter alia, a method of interrupting the execution of a task and servicing an exception in a processor "wherein servicing said exception using said at least one set of exception registers comprises modifying the values of the registers in said set of exception registers without disrupting the state of the interrupted task," as recited in independent claim 11. In particular, the portions of Cohen cited by the Examiner (col. 3, lines 8-28) fail to teach or suggest the exception register allocation called for by such claim language; nor is this deficiency overcome by the remainder of Cohen. Thus, Cohen also cannot anticipate claim 11 under 35 U.S.C. § 102.

The Examiner's basis for this rejection appears to be the statement "and wherein transparent implies w/o disruption of state" (OA, pg. 12, line 2). Again, Applicant respectfully submits that this perfunctory statement by the Examiner fails to establish the development of a clear issue between the Examiner and Applicant (see MPEP § 706.07), and clarification, interview and/or subsequent non-final action is requested. It appears that the Examiner might be arguing that the statement "[f]rom the viewpoint of a user writing software for the CPU, which register set is being used is relatively transparent" (Cohen, col. 3, lines 15-17) somehow corresponds to "wherein servicing said exception using said at least one

set of exception registers comprises modifying the values of the registers in said set of exception registers without disrupting the state of the interrupted task," as recited in independent claim 11. However, this passage from Cohen in no way teaches or suggests any action whatsoever pertaining to the state of the interrupted task. The cited passage simply states that the register access stated in the preceding sentence (indicating either the normal or alternate register is accessed, not both) does not bear consideration to the data access issues contemplated by a software developer. Claim 11, then, is clearly allowable over Cohen, and it is respectfully submitted that the instant rejection also be withdrawn.

## Conclusion

In view of the foregoing remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims. If it is believed that a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (650) 849-6643.

Please grant any extensions of time required to enter this response and charge any additional required fees to deposit account 06-0916.

Respectfully submitted,

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